THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KEVIN J. GEARHARDT
and DARRELL L. PRUEHSNER

Appeal No. 95-0567
Application 07/984,645[1]

ON BRIEF

Before HAIRSTON, JERRY SMITH, and TORCZON, Administrative Patent Judges.

TORCZON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 19, 20, and 21 under 35 U.S.C. § 103.[2]

[1] Application for patent filed 2 December 1992. Appellants claim no priority under 35 U.S.C. §§ 119 or 120.

[2] After the final rejection was entered, the first paragraph of section 103 was redesignated as subsection 103(a). Pub. L. 104-41, sec. 1, 109 Stat. 351 (Nov. 1, 1995).

We reverse.

BACKGROUND

The subject matter of appellants' invention is a scan test apparatus for expanding the capacity of automated test equipment (ATE) for scan-based testing of integrated circuits. (R1[3] at 1.) The scan test apparatus connects to a device under test (DUT) and the ATE. (R1 at 6.) Control vectors are stored in the ATE's memory. The scan test apparatus stores test vectors, including vectors representing the expected test results for comparison. (R1 at 7-9.) The scan test apparatus, under the control of the ATE performing standard tests,[4] loads test vectors into the DUT and receives the DUT's output. The scan test apparatus compares the output against the expected output to generate a pass/fail signal for the ATE. (R1 at 9-10.) The ATE monitors the pass/fail signal to determine whether the DUT is operating correctly. (R1 at 11.)

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[3] Paper 1 from the record.

[4] The word "STANDING" in block 350 of figure 3, which shows the ATE assuming control, should be changed to "STANDARD". See R1 at 10, lines 4, 5, and 8.

Claim 19 defines the invention as follows:

19. A system for testing a scan-based logic integrated circuit device comprising;

a digital tester having a connector for connecting signal lines to at least some external terminals of a device to be tested, and including means for storing control vectors;

a scan test apparatus coupled to said digital tester and to at least one external terminal of said device to be tested, said scan test apparatus including means for storing scan test vectors; and

means operable in said digital tester for enabling said scan test apparatus to download said scan test vectors into said device.

The examiner relied on the following references:

d'Angeac et al.	4,597,042	Jun. 24, 1986
Wilcox et al.	4,996,691	Feb. 26, 1991

Wilcox et al. disclose a digital tester for testing two or more scan-design DUTs. They consider the large quantities of data necessary for a complete test to be a serious problem, so they compare the DUTs against each other (rather than against predicted values) to identify defects. (Cols. 1-2.) Test interfaces for each DUT are linked in series. A master controller controls a control circuit in each interface. The controllers determine whether the input that a DUT receives is the initial test vector or the output of a preceding DUT.

(Cols. 2-3.) The DUT's output is compared against the output of an appropriate preceding DUT to identify variations.[5] (Col. 4.) They do not teach separate storage of test and control vectors. They do suggest the alternative of using additional memory to accommodate large test vectors.

D'Angeac et al. disclose a digital tester for loading test vectors into test circuits for testing scan-design DUTs. (Col. 1.) Test circuits are arranged in parallel to minimize the number of input/output pins. (Col. 3.) A control circuit with a microprocessor and a memory stores the control program and test data. (Col. 5.) They do not teach separate storage of test and control vectors.

DISCUSSION

We have considered, and our opinion presumes familiarity with, the record and the arguments of the examiner and appellants.

Under section 103(a), a claim is only properly rejected if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole

[5] Except for the first DUT, which has no predecessor.

would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. In analyzing a question of obviousness, we must determine the scope and content of the prior art and the differences between the prior art and the claims at issue. Graham v. John Deere Co., 383 U.S. 1, 17 (1966).[6] The invention must be considered as a whole, not piecemeal. Hartness Int'l, Inc. v. Simplimatic Eng'g Co., 819 F.2d 1100, 1108, 2 USPQ2d 1826, 1832 (Fed. Cir. 1987). Similarly, the prior art must be considered as a whole for all it would fairly teach one of ordinary skill in the art. In re Beattie, 974 F.2d 1309, 1311, 24 USPQ2d 1040, 1042 (Fed. Cir. 1992). The examiner bears the burden of establishing a prima facie case by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that one to combine the relevant teachings of the references. The appellants, of course, may demonstrate that no prima facie case

[6] The level of skill in the art and secondary considerations have not been raised as issues in this appeal.

has been properly established. In re Fritch, 972 F.2d 1260, 1265, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992).

The examiner urges that Wilcox provides a basic digital test system with a master controller connected to the DUT. The master controller provides the binary vectors and the means for comparing the test output against the expected output. He relies on d'Angeac for the teaching of a data processing system to store the vectors separately and to download them to the test circuits. (R8 at 2, 4-5; R13 at 4-5.)

Appellants argue that the scan test apparatus "is a separate element not part of the digital tester" and suggest that the examiner has conflated the two. (R12 at 5.) The examiner notes that the claims do not recite separate systems. (R8 at 3.) Consequently, he construes claim 19 to meet the art as follows:

> By combining the two above cited references, the circuit becomes a controller circuit (digital tester) including means with stored control program (control vectors), a means with stored test patterns (test vectors), the control program control which unit to be tested, means to download the data, in means with stored pattern, to the device (circuit under test).

(R13 at 6.) The inquiry, however, is not whether each element existed in the prior art, but whether the prior art made obvious

the invention as a whole. Hartness Int'l at 1108, 2 USPQ2d at 1832. Appellants claim "a scan test apparatus coupled to said digital tester", i.e., two distinct elements. These elements do not have to be separately housed as they are in the embodiments. Amhil Enterp. v. Wawa, Inc., 81 F.3d 1554, 1559, 38 USPQ2d 1471, 1474 (Fed. Cir. 1996) (claims are not limited to the preferred embodiments). However, the prior art must either teach or suggest these elements as distinct (not necessarily physically separated) elements or else the claim limitation will not be met. The examiner has not pointed to a teaching of distinct elements. Nor has he identified a motivation known in the art to separate these elements.

We agree with the examiner that Wilcox suggests the addition of memory to provide a more accurate test. Appellants' argument that Wilcox teaches away because it elects not to use more memory is not persuasive. (R12 at 9.) A reference is relevant for all it fairly teaches about the technology. Fritch at 1264, 23 USPQ2d at 1782; EWP Corp. v. Reliance Universal Inc., 755 F.2d 898, 907, 225 USPQ 20, 25 (Fed. Cir.), cert. denied, 474 U.S. 843 (1985). Wilcox identified a choice between less memory (hence

less expense) and greater accuracy. (Col. 1; R13 at 6.) The fact that Wilcox chose differently than appellants does not negate the teaching. On the other hand, neither Wilcox nor d'Angeac provides a motivation for storing the test and control vectors separately. Moreover, even if the "scan test apparatus" were read to be no more than additional memory,[7] neither reference provides motivation to couple the scan test apparatus directly to the DUT. The rejection cannot be affirmed without a motivation to modify the art. Fritch at 1266, 23 USPQ2d at 1783-84.

Since the rejection of dependent claims 20 and 21 relies on the rejection of independent claim 19, our decision to reverse that rejection extends to the rejection of the dependent claims as well.

[7] No one has analyzed the means-plus-function elements of the claims in light of In re Donaldson Co., 16 F.3d 1189, 1195, 29 USPQ2d 1845, 1850 (Fed. Cir. 1994). Absent such analysis, the scan test apparatus requires only storage means coupled to the digital tester and the DUT. The issue of whether a proper Donaldson analysis would further limit the claims is not before us.

CONCLUSION

The examiner has not satisfied his burden to establish a prima facie case of obviousness with a preponderance of evidence. In particular, the references of record do not teach or suggest a distinct scan test apparatus coupled to a digital tester and to a device under test. Thus, the rejection of claims 19, 20, and 21 under 35 U.S.C. § 103 is

REVERSED

KENNETH W. HAIRSTON)
Administrative Patent Judge)
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JERRY SMITH) BOARD OF PATENT
Administrative Patent Judge) APPEALS
) AND
) INTERFERENCES
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